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Hardware synthesis from encapsulated Verilog modules
- *Smith, D.R.*
Editor(s): Fortes, J., Mongenet, C., Parhi, K.K., Taylor, V.E.
Dept. of Comput. Sci., State Univ. of New York, Stony Brook, NY, USA
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Chicago, IL, USA
1996
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INSPEC Accession Number: 5392654

Abstract:
This paper discusses experience with synthesis from a Verilog writing style us encapsulated modules. The method is shown to be capable of significant adva reduction of code complexity, re-use of submodules, and automatic inference In order to pass synthesis and low level simulation, care must be taken in the of the encapsulated modules through an intermediate style accessible to indu: synthesizers. If the encapsulated modules are edge activated then the control need to be staggered in time through the clock cycle as control is passed dow the hierarchy. Examples are given of a such an intermediate style which is ac synthesis and low level simulation. A conclusion discusses other implications the objective style to hardware design.

Index Terms:
logic design; hardware description languages; computational complexity; infe mechanisms; hardware synthesis; encapsulated Verilog modules; Verilog writ code complexity; automatic inference of control; low level simulation; control clock cycle

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